

Executive Summary

In recent years, the semiconductor industry has begun to experience a significant slowdown in the performance improvements gained from technology scaling. While this is due in part to the impending end of Moore's Law scaling, power consumption has also become a critical limiting factor for the level of performance achievable. The research proposed here aims to enable future generations of computing systems by (1) leveraging an emerging, power-efficient device technology (i.e. the memristor) and (2) considering an alternative architectural model (i.e. neuromorphic) that promises to overcome many of the performance limitations of conventional von Neumann systems. It is worth noting that neuromorphic or neuro-inspired computer architectures are particularly worthwhile given the increasing number of big data problems requiring techniques and systems that can capture knowledge from an abundance of data. Furthermore, it is important to also consider such neuromorphic systems through the lens of the ubiquitous computer systems, including the internet of things (IoT) paradigm and deployable, autonomous systems. Thus, the proposed Reconfigurable and Very Efficient Neuromorphic System (RAVENS) aims to be an energy-efficient neuromorphic architecture specifically tailored for control and other spatio-temporal applications commonly implemented with resource constrained computer systems.

The ultimate objective of this work is to develop approaches that lead to low-power, reconfigurable, high-efficiency brain-inspired computing hardware for embedded control applications, and other applications dealing with dynamic and spatio-temporal data streams. The application domains that frame this work are specifically related to resource constrained systems with limited size, weight, and power (SWaP), necessitating lightweight approaches for implementing brain-inspired, neuromorphic networks. This will be achieved by leveraging our ongoing work on memristive dynamic adaptive neural network arrays (mrDANNA). Building on this effort, we will select optimally performing neuron/synapse configurations (CMOS/memristor circuits) to design and fabricate a fully functional memristive neuromorphic processor capable of efficiently implementing command/control, navigation and avoidance, as well as other spatio-temporal data processing applications. Memristors (or “memory resistors”) are nanoscale electronic switching devices, leveraged here in combination with more conventional CMOS technology to maximize circuit density and reduce overall energy consumption. This effort will provide neuromorphic computing power that meets stringent SWaP metrics for the Air Force that can be leveraged for UAVs, aircraft, satellites, and other deployable autonomous systems.

In our previous efforts we have demonstrated functional CMOS/memristor hybrid circuits that are based on hafnium oxide memristors that have multi-level resistance capability. This multi-level resistance capability is paramount for encoding the synaptic weights in neuromorphic circuits. A key challenge that still needs to be met is to improve memristor performance from the standpoint of reliability and power consumption. To this end, our focus in this effort will be to deliver memristive devices with higher resistance levels (to reduce current drain during operation) and to reduce switch to switch variability to <5%, thus enabling significantly enhanced multi-level switching capability (>10 distinguishable resistance states). These improvements will greatly impact our ability to implement low power neuromorphic computation capable of high accuracy.