



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE  
UNIVERSITY OF TENNESSEE, KNOXVILLE  
FALL 2011 Ph.D. QUALIFYING EXAMINATION  
Monday, August 15, 2011

**Exam Packet Number:** \_\_\_\_\_

**You are allowed 4 hours to complete this exam.**

- This exam is closed book and closed notes. No calculators or cell phones are allowed.
- All your work should be done on the papers that are supplied to you. Do not write on the back of any page. Do not write any answers on this packet!**
- Be sure to put your exam packet number on each sheet that has material to be graded. Do not put your name on any sheet!
- There are 16 equally weighted problems. You are to **SELECT ANY EIGHT** of these to answer. You must make it very clear which eight you choose (see below). If it is not made clear by you, then the first eight problems that you attempt to answer will be graded. Circle only the eight (8) questions that you want graded below:

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### 1. Discrete Structures (CS311)

If and where appropriate, your answers should involve the following concepts: *injective*, *surjective*, *bijective*. If  $z$  is in the domain of relation  $r$ , let  $r(z)$  denote some element such that  $(z, r(z)) \in r$ . Answer the following and include relevant definitions.

- What general condition on  $r$  guarantees  $x = y \Rightarrow r(x) = r(y)$ ?
- What general condition on  $r$  guarantees  $x \neq y \Rightarrow r(x) \neq r(y)$ ?
- What general condition on  $r$  guarantees  $x = y \Leftrightarrow r(x) = r(y)$ ?

### 2. Logic Design (ECE255/CS160)

A multiplexer MUX for two data bits is defined like this:

- MUX has two input data bits  $A, B$ ; one input control bit  $S$ ; and one output bit  $f(S, A, B)$ .
- The MUX output  $f$  equals  $A$  if  $S=0$ ; the output  $f$  equals  $B$  if  $S=1$ .

a) Give the truth table for  $f(S, A, B)$  and write a minimal sum-of-products (MSOP) expression for  $f$ .

b) Use MUXs (with two data inputs as above) to implement a 2-input, 2-output *crossbar switch* which operates like this:

- The crossbar switch has two data input bits  $A, B$ ; a single input control bit  $S$ ; and two data output bits  $Y, Z$ .
- If  $S=0$ , the crossbar connects (or multiplexes)  $A$  to  $Y$  and  $B$  to  $Z$ , while if  $S=1$ , the crossbar connects  $A$  to  $Z$  and  $B$  to  $Y$ .

Draw a logic circuit that implements this crossbar switch using only MUXs (Do not use any other logic gates or functions).

### 3. Calculus (Math)

Is it possible to define  $f(2)$  in a way that extends  $f(x) = \frac{x^2 + x - 6}{x^2 - 4}$  to be continuous at  $x=2$ ? If so,

what value should  $f(2)$  have? Is the function  $g(x) = \frac{\sin x}{x}$  continuous at  $x=0$ ? What is the limit of

$\frac{\sin x}{x}$  as  $x$  tends to zero (i.e.,  $x \rightarrow 0$ )? Is it possible to extend the function  $g(x)$  to be continuous at  $x=0$ ?

### 4. Programming (ECE206/CS102)

Write a computer program (in any language) to calculate, without using any functions from a math library (such as *sqrt*) the square root of 2.0, accurate to at least one part in 10, 000. The program is to print this value to the standard output.

### 5. Probability and Random Variables (ECE313)

Let  $X$  and  $Y$  be independent random variables that take values in the set  $\{1, 2, 3\}$ . Let  $V = 2X + 2Y$  and  $W = X - Y$ . Assume that  $P(X=k)$  and  $P(Y=k)$  are positive for any  $k$  in the set  $\{1, 2, 3\}$ . Can  $V$  and  $W$  be independent? Explain your answer (no calculations are needed).

## 6. Computer Architecture (ECE355/ECE451/CS160)

(a) Indicate whether the following statements are true or false by circling the correct answer.

- |      |       |  |
|------|-------|--|
| TRUE | FALSE | The 'principle of locality' refers to cache memory being physically closer to the CPU than main memory.      |
| TRUE | FALSE | In an inclusive multi-level cache, L1 may contain data not found in L2.                                      |
| TRUE | FALSE | A direct mapped cache typically employs an LRU replacement policy.   |
| TRUE | FALSE | An n-way set-associative cache is a compromise between strictly associative and direct mapped cache designs. |
| TRUE | FALSE | An L1 cache is typically smaller, but also faster than an L2 cache.  |

(b) A computer has a two-level cache. Suppose that 60% of the memory references hit on level 1, 30% hit on level 2 and 10% miss all together and go to main memory. The access times are 2ns, 10ns, and 40ns, respectively, where the times for the level 2 cache and main memory first start counting at the moment it is known that they are needed. Also, it takes equally long to determine cache hits and misses.

What is the average access time? Express first the weighted sum with all its terms, then give the numerical answer.

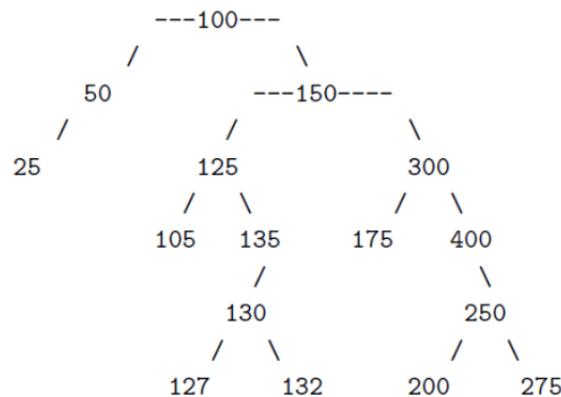
## 7. Data Structures (CS140)

Answer all three parts of this question and assume that for all three parts you are dealing with an unbalanced, binary search tree.

a. Show the binary search tree that results from the following sequence of insertions:

80, 60, 55, 90, 150, 70, 110, 85, 115.

b. Show the binary search tree that results if 150 is deleted from the tree below:



c. What is the worst case insertion time for an unbalanced, binary search tree? Express your answer using Big-O notation and assume that n elements are inserted into the tree. What circumstances cause this worst case insertion time to occur?

## 8. Algorithms (CS302)

a. What is Dijkstra's shortest path algorithm, and exactly how does it work?

b. What is the running time of each step?

c. Illustrate how it works using the following example:

$V = \{A, B, C, D\}$

$E = \{(A, B, 9), (A, C, 18), (B, D, 15), (C, D, 5)\}$

A = Starting node

D = Ending node

### 9. Operating Systems (CS360)

Describe the effectiveness of the following scheduling policies and blend of jobs. In each, explain the way in which the policy is effective and the way in which is is ineffective. Use proper performance metrics.

- First-Come-First-Serve scheduling with 5 CPU-bound jobs.
- Round robin scheduling with 5 CPU-bound jobs.
- Round robin scheduling with 10 CPU-bound and 3 I/O bound jobs.
- Predictive SJF scheduling with 10 CPU-bound and 3 I/O bound jobs.

Assume that the CPU-bound jobs have large, roughly equal but finite CPU burst times followed by a short I/O burst. The I/O bound jobs have bursts of I/O interspersed with very short CPU bursts.

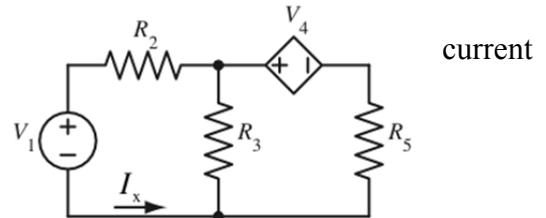
### 10. Linear Algebra (Math)

Assume that matrices A and B are positive definite. Then, is their product, AB, positive definite? If yes, prove it. If no, give a counter example.

### 11. Circuits (ECE300)

In the circuit below the voltage  $V_4$  in volts is  $k$  times the the  $I_x$  in amps. What value of  $k$  will minimize the power delivered to resistor  $R_3$ ?

$$V_1 = 10V, R_2 = 15\Omega, R_3 = 50\Omega, R_5 = 10\Omega$$



### 12. Signals & Systems (ECE315/316)

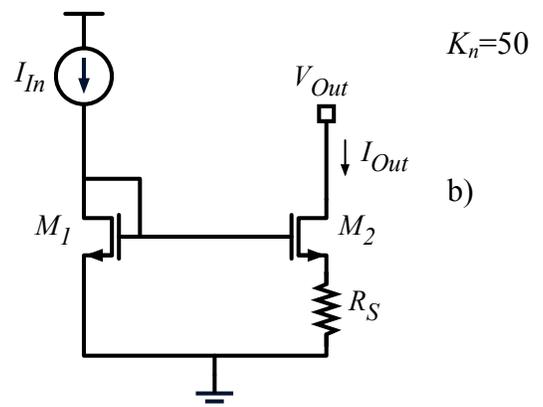
A continuous-time system with transfer function  $H(s) = \frac{s+2}{s(s+8)}$  is excited by a unit impulse  $x(t) = \delta(t)$ . The response is  $h(t)$ . At what time  $t$  (in seconds) does the response equal 80% of its maximum value?

### 13. Electronics

Consider the NMOS Widlar current source shown at right.  $\mu A/V^2, V_{Th} = 0.6 V, \lambda = .025 V^{-1}$ .

a) If  $I_m = 100 \mu A$ , find the value for  $R_S$  such that  $I_{Out} = 25 \mu A$ . Neglect channel-length modulation and assume  $M_2$  is in saturation for this part.

What is the minimum value of  $V_{Out}$  for which this current source operates correctly?



$$K_n = 50$$

b)

#### 14. Power (ECE325)

A three-phase, balanced induction machine is connected to rated supply. The synchronous speed of this machine is 1800 rpm. The parameters of its Thevenin equivalent circuit (for one-phase) under rated supply is given as:

$$V_{th}=250 \text{ V}, R_{th}=0.10 \Omega, X_{th}=0.30 \Omega, R'_2=0.05 \Omega, X'_2=0.35 \Omega$$

Determine:

- 1) Draw the Thevenin equivalent circuit (for one-phase).
- 2) The maximum torque that the machine can develop.
- 3) The speed at which the maximum torque is developed.
- 4) The startup torque.
- 5) The external resistance required in each rotor phase, if the maximum torque is to occur at start.

Assume a turns ratio (stator to rotor) of 1.5.

Needed equations (for one-phase):

$$\omega_{syn} = n_s \frac{2\pi}{60}, T_{mech} = \frac{1}{\omega_{syn}} \frac{V_{th}^2}{(R_{th} + R'_2/s)^2 + (X_{th} + X'_2)^2} \frac{R'_2}{s}$$

$$s_{T_{max}} = \frac{R'_2}{\sqrt{R_{th}^2 + (X_{th} + X'_2)^2}}, T_{max} = \frac{1}{2\omega_{syn}} \cdot \frac{V_{th}^2}{R_{th} + \sqrt{R_{th}^2 + (X_{th} + X'_2)^2}}$$

#### 15. Electromagnetics (ECE341) (Smith Chart allowed)

A voltage wave of 5 V (rms) at 1 GHz is incident to a 50  $\Omega$  lossless transmission line. The line is  $0.6\lambda$  long and is terminated by  $Z_L = (30 - j40) \Omega$ . Obtain

- a) The reflection coefficient and the voltage standing wave ratio **at the input side**; and the impedance  $Z_{in}$  looking into the input side of the line.
- b) The distance of the first minimum voltage **from the load**
- c) Use single stub matching and determine the location of a shunt stub, and its length for proper matching at 1 GHz.
- d) Power delivered to the load before and after matching.

#### 16. Communications (ECE342)

Define, explain or answer the following:

- a. Consider modulation schemes of AM, DSB, and PM. Which one is most generally likely to have the best immunity to adjacent channel interference?
- b. Why can FM have greater interference immunity than that of PM? Be specific.
- c. Under what conditions does an envelope detector yield about the same signal-to-noise ratio to that of a synchronous detector?
- d. What is the adverse consequence if an envelope detector is used when the signal to noise ratio is relatively low?
- e. Why does PM have limited ability for increases in destination SNR?
- f. Draw a circuit that models a resistor as a noise source.
- g. What type of linear modulation would you choose if you have to transmit a message with significant DC content?
- h. Consider a digital system being operated in a noisy environment where a logic zero is represented by -5 volts and a logic 1 is represented by a +5 volts. What would be the optimum threshold point (in volts)?